



US Patent & Trademark Office

[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

 Search: ☒ The ACM Digital Library ☐ The Guide



THE ACM DIGITAL LIBRARY


[Feedback](#) [Report a problem](#) [Satisfaction survey](#)

Terms used

cpu and register and accelerator and java and execute

Found 21,882 of 123,929

 Sort results
by


[Save results to a Binder](#)
[Try an Advanced Search](#)
[Try this search in The ACM Guide](#)

 Display
results


[Search Tips](#)
☐ Open results in a new window

Results 1 - 20 of 200

Result page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [next](#)

Best 200 shown

Relevance scale ☐ ☐ ☐ ☐ ☐

1 [Improving Java performance using hardware translation](#)

Ramesh Radhakrishnan, Ravi Bhargava, Lizy K. John

June 2001 **Proceedings of the 15th international conference on Supercomputing**

Full text available: pdf(254.91 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

State of the art Java Virtual Machines with Just-In-Time (JIT) compilers make use of advanced compiler techniques, run-time profiling and adaptive compilation to improve performance. However, these techniques for alleviating performance bottlenecks are more effective in long running workloads, such as server applications. Short running Java programs, or client workloads, spend a large fraction of their execution time in compilation instead of useful execution when run using JIT compilers. In ...

2 [A survey of processors with explicit multithreading](#)

Theo Ungerer, Borut Robič, Jurij Silc

March 2003 **ACM Computing Surveys (CSUR)**, Volume 35 Issue 1

Full text available: pdf(920.16 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Hardware multithreading is becoming a generally applied technique in the next generation of microprocessors. Several multithreaded processors are announced by industry or already into production in the areas of high-performance microprocessors, media, and network processors. A multithreaded processor is able to pursue two or more threads of control in parallel within the processor pipeline. The contexts of two or more threads of control are often stored in separate on-chip register sets. Unused i ...

Keywords: Blocked multithreading, interleaved multithreading, simultaneous multithreading

3 [Architectures: 3D graphics LSI core for mobile phone "Z3D"](#)

Masatoshi Kameyama, Yoshiyuki Kato, Hitoshi Fujimoto, Hiroyasu Negishi, Yukio Kodama, Yoshitsugu Inoue, Hiroyuki Kawai

July 2003 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS conference on Graphics hardware**

Full text available: pdf(649.83 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#)

In this paper we describe the architecture of the 3D graphics LSI core for mobile phone

[IEEE HOME](#) | [SEARCH IEEE](#) | [SHOP](#) | [WEB ACCOUNT](#) | [CONTACT IEEE](#)[Membership](#) | [Publications/Services](#) | [Standards](#) | [Conferences](#) | [Careers/Jobs](#)**IEEE Xplore**
RELEASE 1.5Welcome
United States Patent and Trademark Office[Help](#) | [FAQ](#) | [Terms](#) | [IEEE Peer Review](#)[Quick Links](#)» [See](#)

Welcome to IEEE Xplore®

Your search matched **[0]** of **[987065]** documents.

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

[Print Format](#)

You may refine your search by editing the current search expression or entering a new one the text box. Then click search Again.

java and execute and accelerator and cpu and bytec

[Search Again](#)**OR**

Use your browser's back button to return to your original search page.

Results:

No documents matched your query.

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#)
[Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#)
[No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2003 IEEE — All rights reserved

WEST[Help](#)[Logout](#)[Interrupt](#)[Main Menu](#)[Search Form](#)[Posting Counts](#)[Show S Numbers](#)[Edit S Numbers](#)[Preferences](#)[Cases](#)**Search Results -**

Terms	Documents
l13 and sipush and bipush	9

Database:

US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search:

L16

[Refine Search](#)[Recall Text](#)[Clear](#)**Search History****DATE:** **Monday, November 24, 2003** [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

Hit Count Set Name

result set

*DB=USPT; PLUR=YES; OP=ADJ*L16 l13 and sipush and bipush9 L16L15 L14 and (mark\$ near5 variable\$)0 L15L14 L13 and accelerator\$13 L14*DB=USPT,TDBD; PLUR=YES; OP=ADJ*L13 l2 and overflow and underflow17 L13*DB=USPT; PLUR=YES; OP=ADJ*L12 l7 and overflow and underflow0 L12*DB=TDBD; PLUR=YES; OP=ADJ*L11 cpu and register and processor\$ and ((translat\$ or convert\$) near5 instruction\$) and (execut\$ near5 java)0 L11*DB=DWPI; PLUR=YES; OP=ADJ*L10 cpu and register and processor\$ and ((translat\$ or convert\$) near5 instruction\$) and (execut\$ near5 java)0 L10*DB=EPAB; PLUR=YES; OP=ADJ*L9 cpu and register and processor\$ and ((translat\$ or convert\$) near5 instruction\$) and (execut\$ near5 java)0 L9*DB=JPAB; PLUR=YES; OP=ADJ*L8 cpu and register and processor\$ and ((translat\$ or convert\$) near5 instruction\$) and (execut\$ near5 java)0 L8*DB=PGPB; PLUR=YES; OP=ADJ*L7 cpu and register and processor\$ and ((translat\$ or convert\$) near5 instruction\$) and (execut\$ near5 java)50 L7*DB=USPT; PLUR=YES; OP=ADJ*L6 ((711/1 |711/108)!.CCLS.)559 L6L5 ((712/202 |712/36 |712/229)!.CCLS.)487 L5L4 L3 and l210 L4L3 ((717/136 |717/137 |717/138 |717/139 |717/140 |717/118 |717/143 |717/148)!.CCLS.)716 L3L2 cpu and register and processor\$ and ((translat\$ or convert\$) near5 instruction\$) and (execut\$ near5 java)51 L2L1 cpu and register and processor and ((translat\$ or convert\$) near5 instruction\$) and (exect\$ near5 java)0 L1

END OF SEARCH HISTORY